WHAT IS CLAIMED IS:

1. A reconfigurable memory comprising:

M bit lines, where M>1;

a plurality of row lines;

an array of memory storage cells, each memory storage cell storing a data value and comprising circuitry for coupling that data value to one of said bit lines in response to a row control signal on one of said row lines;

a row select circuit for generating said row control signal on one of said row lines in response to a row address being coupled to said row select circuit, said row select circuit comprising a memory for storing a mapping of said row addresses to said row lines, said mapping determining which of said row lines is selected for each possible value of said row address; and

a controller for determining that one of said memory cells is defective and for altering said mapping to eliminate references to that row line that causes that defective storage cell to couple a data value to one of said bit lines.

2. The reconfigurable memory of Claim 1 wherein said controller tests all of said memory storage cells to determine if any of said memory storage cells is defective each time power is applied to said controller and wherein said controller eliminates references in said mapping to row lines that cause said detected defective storage cells to couple data values to said bit lines.

3. The reconfigurable memory of Claim 2 wherein said controller assigns a row address to each of said reference lines that was not eliminated because of a defective memory cell and

wherein said controller communicates the maximum number of rows available for storing data values after the elimination of said defective row references.

4. The reconfigurable memory of Claim 1 wherein said memory further comprises a single cell memory for storing a plurality of single data values, each data value corresponding to one of said row addresses and one of said bit lines and wherein said controller further comprises a circuit for causing that data value stored in said single cell memory for one of said row addresses and bit lines to replace that value stored in said memory storage cell coupled to that bit line when that row address is coupled to said row select circuit.

5. The reconfigurable memory of Claim 1 further comprising a word assembly circuit for selecting N bit lines from said M bit lines, where N is less than or equal to M, said word assembly circuit comprising a memory for storing a mapping specifying said N bit lines for each possible row address, wherein said controller alters said mapping to eliminate a reference in said mapping to a bit line that causes a defective storage cell to couple data to a bit line in response to one of said row addresses.

6. The reconfigurable memory of Claim 5 wherein said word assembly circuit comprises a cross-connect switch for coupling said M bit lines to N data lines.

7. The reconfigurable memory of Claim 6 wherein said cross-connect switch is partially populated such that only selected ones of said M bit lines can be connected to any particular data line.

8. The reconfigurable memory of Claim 1 further comprising an error correcting circuit for detecting errors in data words, said error correcting circuit generating a corrected data word and an error data word from N data values coupled thereto, said error data word indicating which of said N data values, if any, was erroneous; and

a word assembly circuit for connecting N of said M bit lines to said error correcting circuit, where N is less than or equal to M; wherein said control circuit is connected to said error correcting circuit and receives said error data words and said row addresses, said control circuit altering said mapping in said row select circuit in response to said error data words.

9. The memory of Claim 8 wherein N<M and wherein said word assembly circuit comprises a cross-connect circuit for connecting N of said M bit lines to said error correcting circuit.

10. The memory of Claim 8 further comprising an error correcting code generating circuit for generating an error correcting data word from a data word, said error correcting data word being stored in a location corresponding to said data word in said memory.

11. The memory of Claim 10, wherein said error correcting data word is stored in the same row of memory cells as said data word used to generate said error correcting data word.